Keysight N6470A Thunderbolt 3 Electrical Compliance Test Application

KEYSIGHT TECHNOLOGIES

Programmer's Reference

Notices

Revision

Version 01.00.0000

Edition

June 21, 2016

Available in electronic format only

Published by:
Keysight Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

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In This Book

This book is your guide to programming the Keysight Technologies N6470A Thunderbolt 3 Electrical Compliance Test Application.

- Chapter 1, “Introduction to Programming,” starting on page 7, describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 19, and Chapter 4, “Instruments,” starting on page 57, provide information specific to programming the N6470A Thunderbolt 3 Electrical Compliance Test Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, and 4 for changes.

Contents

1 Introduction to Programming

Remote Programming Toolkit / 8

This chapter introduces the basics for remote programming a compliance application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The N6470A Thunderbolt 3 Electrical Compliance Test Application uses Remote Interface Revision 3.50. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

2 Configuration Variables and Values

The following table contains a description of each of the N6470A Thunderbolt 3 Electrical Compliance Test Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"
```

```
C# syntax
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Configure	ACCM Acquisition Number	ACCMAcqNum	(Accepts user-defined text), 1, 5, 10, 15	Select the number of signal acquisitions for live signal analysis (Signal Acquisition Method = [Live]) of AC Common Mode tests.
Configure	Acquisition Bandwidth	RiseFallTimeAcqBW	AUTO, AcquisitionSetup	Select the acquisition bandwidth for the rise/fall time measurement. For [Auto], the acquisition bandwidth will be set to maximum (Automatic). For [Acquisition Setup], the acquisition bandwidth will be set to the value based on the settings in Tools->Acquisition Setup.
Configure	Automation Timeout	AutomationTimeout	(Accepts user-defined text), 200	Select the controller automation timeout. Unit : second.
Configure	Average Number	EquAvgNum	Max, 2, 4, 16, 64, 256, 1024, 4096, 16384, 65534	Select the averaging number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of equalization test. Select [Max] for maximum averaging number of the oscilloscope.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Equalization Coefficient Automation	EnableEquCoefficientAutomation	Enable, Disable	Select to enable or disable the equalization coefficient (C0 and C1) increament and decreament automation.
Configure	Equalization Coefficient Step	EquCoefficientStep	(Accepts user-defined text), 1	Select the equalization coefficient (C0 and C1) increament and decreament step.
Configure	Eye Mask Acquisition Number	MaskAcqNum	(Accepts user-defined text), 1, 5, 10, 15	Select the number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of mask test.
Configure	Eye Mask Horizontal Shift Step Number	MaskHorShiftStepNum	(Accepts user-defined text), 2, 5, 9, 10, 20	Select the number of steps by which the mask must be shifted horizontally through one entire unit interval when the mask fails.
Configure	ISI Filter Lagging Bit	ISILagBit	0.0, 1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0, 14.0, 15.0	Select a value for the lagging/trailing bit, which is used to calculate the ISI filter. This config is only applicable when the Jitter Pattern Length value is set to [Arbitrary]. The lagging/trailing bit is greater than or equal to 0.
Configure	ISI Filter Leading Bit	ISILeadBit	0.0, -1.0, -2.0, -3.0, -4.0, -5.0, -6.0, -7.0, -8.0, -9.0, -10.0	Select a value for the leading bit, which is used to calculate the ISI filter. This config is only applicable when the Jitter Pattern Length value is set to [Arbitrary]. The leading bit is less than or equal to 0.
Configure	Interpolation Point	InterpolationPoint	OFF, ON, INT1, INT2, INT4, INT8, INT16	Select the Sin(x)/x interpolation point for acquiring the waveform for all Thunderbolt tests.
Configure	Jitter Pattern Length	JitterPLength	Default, ARBitrary, AUTO	Select the type of pattern length used for RjDj measurement. For [Default] Jitter Pattern Length, Periodic algorithm will be used for patten length less than 4096; Arbitrary algorithm will be used for others.
Configure	Lane 0 Connection	L0Connection	5	Select the input channel for the Lane 0.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Lane 1 Connection	L1Connection	6	Select the input channel for the Lane 1.
Configure	Pattern Check	EnableSignalCheck	1.0, 0.0	When pattern check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Configure	RJ Bandwidth	RJBandwidth	NARRow, WIDE	Select the type of filter bandwidth used to separate the DDJ from the RJ and PJ.
Configure	RJ Method	RJMethod	BOTH, SPECtral	Select the type of method used to separate the RJ component.
Configure	SSC Filter Window Size	SSC_LPF_WindowSize	(Accepts user-defined text), 0, 900, 1000, 2000, 3000, 4000, 5000	Select the Moving Average Filter's window size used to separate the SSC profile for Unit Interval and SSC measurement.
Configure	SSC Phase Acquisition Number	SSCPhaseAcqNum	(Accepts user-defined text), 1, 5, 10, 15	Select the number of signal acquisition for live signal analysis (Signal Acquisition Method = [Live]) of SSC Phase tests.
Configure	SSC Phase LPF Bandwidth	SSCPhaseLPFBandwidth	1.0E+6, 2.0E+6, 3.0E+6, 4.0E+6, 5.0E+6, 6.0E+6, 7.0E+6, 8.0E+6	Select the bandwidth for the 2nd order Low-Pass Filter (LPF) used to filter on the signal phase jitter. Unit : MHz.
Configure	SSC Phase LPF Damping Factor	SSCPhaseLPFDampFactor	(Accepts user-defined text), 0.570, 0.580, 0.707, 1.250, 1.750	Select the damping factor for the 2nd order Low-Pass Filter (LPF) used to filter on the signal phase jitter.
Configure	Sample Size - All Pattern (Live)	SampSize_MemPts_Live	(Accepts user-defined text), 8.0, 10.0, 20.0, 40.0	Select the memory points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]), except Unit Interval and SSC tests. Unit : Mpts.
Configure	Sample Size - SSC Phase (Live)	SampSize_MemPts_SSCPhase_Live	(Accepts user-defined text), 8.0, 10.0, 20.0, 40.0	Select the memory points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of SSC Phase tests. Unit : Mpts.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Sample Size - Unit Interval and SSC Modulation (Live)	SampSize_MemPts_UI_SSC_Live	(Accepts user-defined text), 8.0, 10.0, 20.0, 26.0, 40.0	Select the memory points used for acquiring signal for live signal analysis (Signal Acquisition Method = [Live]) of Unit Interval and SSC Modulation tests. Unit : Mpts.
Configure	Sampling Rate	SampRate	80.0E9, 40.0E9	Select the sampling rate taht must be used to acquire the waveform(s) for all Thunderbolt tests. Unit: Sa/s.
Configure	Screenshot Image Size	ScreenShotImageSize	GRAT, SCR	Select the screenshot image size for the report items.
Configure	Signal Acquisition Method	SigAcqMethod	Live, Save_Waveform	Select the signal acquisition method. Select [Live] for live signal analysis without saving the signal waveform. Select [Save Waveform] for memory signal analysis (Live signal is saved prior analysis).
Configure	Signal Trigger Level	TriggerThreshold	(Accepts user-defined text), 0.0, 50.0E-03, 100.0E-03, 150.0E-03, 200.0E-03, 250.0E-03, 300.0E-03, 350.0E-03, 400.0E-03, 450.0E-03, 500.0E-03, 550.0E-03, 600.0E-03	Choose the trigger level for all the signal in Thunderbolt tests. Unit: volt.
Configure	Skew Time Tolerance	SkewTimeTolerance	(Accepts user-defined text), 3.00, 20.0, 40.0, 48.485, 50.0, 96.970	Select the time difference allowed for skew time measurement. Time difference greater than tolerance will be ignored. Default value is set to half of the UI. Unit: ps.
Configure	Tx Equalization Preset	TxEqualization_Preset	ALL, P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Select ALL for all Preset numbers or select specific Preset number to test.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Tx TBT_CDR1 Bandwidth	TxCDR1Bandwidth	1.0E+6, 2.0E+6, 3.0E+6, 4.0E+6, 5.0E+6, 6.0E+6, 7.0E+6, 8.0E+6	Select the bandwidth for the Thunderbolt CDR1 (2nd order PLL) used in clock-to-data-recovery for transmitter test. Unit : MHz.
Configure	Tx TBT_CDR1 Damping Factor	TxCDR1DampFactor	(Accepts user-defined text), 0.570, 0.580, 0.707, 1.250, 1.750	Select the damping factor for the Thunderbolt CDR1 (2nd order PLL) used in clock-to-data-recovery for transmitter test.
Configure	Tx TBT_CDR2 Bandwidth	TxCDR2Bandwidth	1.0E+6, 2.0E+6, 3.0E+6, 4.0E+6, 5.0E+6, 6.0E+6, 7.0E+6, 8.0E+6	Select the bandwidth for the Thunderbolt CDR2 (2nd order PLL) used in clock-to-data-recovery for transmitter test. Unit : MHz.
Configure	Tx TBT_CDR2 Damping Factor	TxCDR2DampFactor	(Accepts user-defined text), 0.570, 0.580, 0.707, 1.250, 1.750	Select the damping factor for the Thunderbolt CDR2 (2nd order PLL) used in clock-to-data-recovery for transmitter test.
Configure	Unit Interval Mean Filter Window Size	UI_LPF_WindowSize	(Accepts user-defined text), 0, 900, 1000, 2000, 3000, 4000, 5000	Select the Moving Average Filter's window size used for Unit Interval mean measurement.
Configure	Unit Interval Mean Window Count	UI_WindowCount	Max, 10, 20, 50, 100	Select the number of windows used for Unit Interval mean measurement.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 100	Specify N using the 'Minimum required margin %' control.
Set Up	Bit Rate	BitRate	10.3125 GB/s, 20.625 GB/s	Select the bit rate for the compliance tests. Select the bit rate for the compliance tests.
Set Up	Crosstalk Instrument	CrosstalkInstrument	None, JBERTB_IP, JBERTB_SICL, JBERTA_IP, JBERTA_SICL	Setup the external instrument used for crosstalk during remote interface. Setup the external instrument used for crosstalk during remote interface.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	DUT Type	DUTType	Device, Host	Set the DUT type to either Device or Host. Set the DUT type to either Device or Host.
Set Up	Device Identifier	DeviceIdentifier	(Accepts user-defined text), (Select or Type)	Identifier for the DUT in testing. Identifier for the DUT in testing.
Set Up	Enable Controller	AutomationEnable	0.0, 1.0	Enable or disable the use of Thunderbolt Micro-Controller. Enable or disable the use of Thunderbolt Micro-Controller.
Set Up	Enable Controller	ControllerEnable	0.0, 1.0	Enable or disable the use of Thunderbolt Micro-Controller. Enable or disable the use of Thunderbolt Micro-Controller.
Set Up	Enable Saved Waveform	SavedWaveformEnable	0.0, 1.0	Enable or disable the use of saved waveform in the tests. Enable or disable the use of saved waveform in the tests.
Set Up	IP Address	IPAddress	(Accepts user-defined text)	IP address of the external instrument used for crosstalk during remote interface. IP address of the external instrument used for crosstalk during remote interface.
Set Up	PRBS11_NegSignal Directory	PRBS11_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS11 negative signal waveform. This variable use to store the directory of PRBS11 negative signal waveform.
Set Up	PRBS11_PosSignal Directory	PRBS11_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS11 positive signal waveform. This variable use to store the directory of PRBS11 positive signal waveform.
Set Up	PRBS31_NegSignal Directory	PRBS31_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS31 negative signal waveform. This variable use to store the directory of PRBS31 negative signal waveform.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	PRBS31_PosSignal Directory	PRBS31_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS31 positive signal waveform. This variable use to store the directory of PRBS31 positive signal waveform.
Set Up	PRBS9_NegSignalD irectory	PRBS9_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS9 negative signal waveform. This variable use to store the directory of PRBS9 negative signal waveform.
Set Up	PRBS9_PosSignalD irectory	PRBS9_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of PRBS9 positive signal waveform. This variable use to store the directory of PRBS9 positive signal waveform.
Set Up	Port Number	PortNumber	1 Port, 2 Ports	Set the number of ports for the DUT. Set the number of ports for the DUT.
Set Up	Port1 Name	Port1Name	(Accepts user-defined text), Port 1, (Select or Type)	Set the port name for the first port. This field will be show in report. Set the port name for the first port. This field will be show in report.
Set Up	Port2 Name	Port2Name	(Accepts user-defined text), Port 2, (Select or Type)	Set the port name for the second port. This field will be show in report. Set the port name for the second port. This field will be show in report.
Set Up	PresetNumber	cfgPresetNumber	(Accepts user-defined text), P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15	Set the Preset Number. This field will be show in report. Set the Preset Number. This field will be show in report.
Set Up	SQ2_NegSignalDire ctory	SQ2_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ2 negative signal waveform. This variable use to store the directory of SQ2 negative signal waveform.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	SQ2_PosSignalDirectory	SQ2_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ2 positive signal waveform. This variable use to store the directory of SQ2 positive signal waveform.
Set Up	SQ_NegSignalDirectory	SQ_Neg_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ16/SQ32 negative signal waveform. This variable use to store the directory of SQ16/SQ32 negative signal waveform.
Set Up	SQ_PosSignalDirectory	SQ_Pos_wfm	(Accepts user-defined text)	This variable use to store the directory of SQ16/SQ32 positive signal waveform. This variable use to store the directory of SQ16/SQ32 positive signal waveform.
Set Up	Sicl Address	SiclAddress	(Accepts user-defined text)	Sicl address of the external instrument used for crosstalk during remote interface. Sicl address of the external instrument used for crosstalk during remote interface.
Set Up	Specification version	SpecVersion	Specification Rev 3.0	Select the test specification for testing. Select the test specification for testing.
Set Up	Test Lane Port 1	TestLanePort1	Both lanes, Lane 0 only, Lane 1 only	Select the test lane of Port 1 for testing. Select the test lane of Port 1 for testing.
Set Up	Test Lane Port 2	TestLanePort2	Both lanes, Lane 0 only, Lane 1 only	Select the test lane of Port 2 for testing. Select the test lane of Port 2 for testing.
Set Up	User Comments	UserComments	(Accepts user-defined text)	Additional comments for the DUT. Additional comments for the DUT.
Set Up	User Description	UserDescription	(Accepts user-defined text), (Select or Type)	Short description for the DUT. Short description for the DUT.

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application:

NOTE The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
1.1.0 Tx Lane Intra-pair Output Skew (Port 1, Lane 0)	2101	The Tx lane intra-pair output skew at TP1 of a Thunderbolt device must be less than maximum limit. The lane intra-pair output skew measurement is the time difference between the single-ended mid-point of the Tx+ signal rising/falling edge, and the single-ended mid-point of the Tx- signal falling/rising edge.
1.1.0 Tx Lane Intra-pair Output Skew (Port 1, Lane 0)	1101	The Tx lane intra-pair output skew at TP1 of a Thunderbolt host must be less than maximum limit. The lane intra-pair output skew measurement is the time difference between the single-ended mid-point of the Tx+ signal rising/falling edge, and the single-ended mid-point of the Tx- signal falling/rising edge.
1.1.0 Tx Lane Intra-pair Output Skew (Port 1, Lane 1)	2201	The Tx lane intra-pair output skew at TP1 of a Thunderbolt device must be less than maximum limit. The lane intra-pair output skew measurement is the time difference between the single-ended mid-point of the Tx+ signal rising/falling edge, and the single-ended mid-point of the Tx- signal falling/rising edge.
1.1.0 Tx Lane Intra-pair Output Skew (Port 1, Lane 1)	1201	The Tx lane intra-pair output skew at TP1 of a Thunderbolt host must be less than maximum limit. The lane intra-pair output skew measurement is the time difference between the single-ended mid-point of the Tx+ signal rising/falling edge, and the single-ended mid-point of the Tx- signal falling/rising edge.
1.1.0 Tx Lane Intra-pair Output Skew (Port 2, Lane 0)	2301	The Tx lane intra-pair output skew at TP1 of a Thunderbolt device must be less than maximum limit. The lane intra-pair output skew measurement is the time difference between the single-ended mid-point of the Tx+ signal rising/falling edge, and the single-ended mid-point of the Tx- signal falling/rising edge.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.0 Tx Lane Intra-pair Output Skew (Port 2, Lane 0)	1301	The Tx lane intra-pair output skew at TP1 of a Thunderbolt host must be less than maximum limit. The lane intra-pair output skew measurement is the time difference between the single-ended mid-point of the Tx+ signal rising/falling edge, and the single-ended mid-point of the Tx- signal falling/rising edge.
1.1.0 Tx Lane Intra-pair Output Skew (Port 2, Lane 1)	2401	The Tx lane intra-pair output skew at TP1 of a Thunderbolt device must be less than maximum limit. The lane intra-pair output skew measurement is the time difference between the single-ended mid-point of the Tx+ signal rising/falling edge, and the single-ended mid-point of the Tx- signal falling/rising edge.
1.1.0 Tx Lane Intra-pair Output Skew (Port 2, Lane 1)	1401	The Tx lane intra-pair output skew at TP1 of a Thunderbolt host must be less than maximum limit. The lane intra-pair output skew measurement is the time difference between the single-ended mid-point of the Tx+ signal rising/falling edge, and the single-ended mid-point of the Tx- signal falling/rising edge.
1.1.0a Preset Calibration (Port 1, Lane 0)	1810	The Preset Calibration is used to find the optimized preset for the platform.
1.1.0a Preset Calibration (Port 1, Lane 0)	2810	The Preset Calibration is used to find the optimized preset for the platform.
1.1.0a Preset Calibration (Port 1, Lane 1)	1811	The Preset Calibration is used to find the optimized preset for the platform.
1.1.0a Preset Calibration (Port 1, Lane 1)	1813	The Preset Calibration is used to find the optimized preset for the platform.
1.1.0a Preset Calibration (Port 1, Lane 1)	2811	The Preset Calibration is used to find the optimized preset for the platform.
1.1.0a Preset Calibration (Port 1, Lane 1)	2813	The Preset Calibration is used to find the optimized preset for the platform.
1.1.0a Preset Calibration (Port 2, Lane 0)	1812	The Preset Calibration is used to find the optimized preset for the platform.
1.1.0a Preset Calibration (Port 2, Lane 0)	2812	The Preset Calibration is used to find the optimized preset for the platform.
1.1.0b CTLE Calibration (Port 1, Lane 0)	1820	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.1.0b CTLE Calibration (Port 1, Lane 0)	2820	The CTLE Calibration is used to find the optimized DC gain value for the platform.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.0b CTLE Calibration (Port 1, Lane 1)	1821	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.1.0b CTLE Calibration (Port 1, Lane 1)	1823	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.1.0b CTLE Calibration (Port 1, Lane 1)	2821	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.1.0b CTLE Calibration (Port 1, Lane 1)	2823	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.1.0b CTLE Calibration (Port 2, Lane 0)	1822	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.1.0b CTLE Calibration (Port 2, Lane 0)	2822	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.1.1 Tx Rise Time (Port 1, Lane 0)	2111	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.1 Tx Rise Time (Port 1, Lane 0)	1111	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.1 Tx Rise Time (Port 1, Lane 1)	2211	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.1 Tx Rise Time (Port 1, Lane 1)	1211	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.1 Tx Rise Time (Port 2, Lane 0)	2311	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.1 Tx Rise Time (Port 2, Lane 0)	1311	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.1 Tx Rise Time (Port 2, Lane 1)	2411	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.1 Tx Rise Time (Port 2, Lane 1)	1411	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.10a Tx Unit Interval, Min (Port 1, Lane 0)	2151	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.1.10a Tx Unit Interval, Min (Port 1, Lane 0)	1151	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.1.10a Tx Unit Interval, Min (Port 1, Lane 1)	2251	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.1.10a Tx Unit Interval, Min (Port 1, Lane 1)	1251	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.1.10a Tx Unit Interval, Min (Port 2, Lane 0)	2351	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.1.10a Tx Unit Interval, Min (Port 2, Lane 0)	1351	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.1.10a Tx Unit Interval, Min (Port 2, Lane 1)	2451	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.1.10a Tx Unit Interval, Min (Port 2, Lane 1)	1451	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.1.10b Tx Unit Interval, Max (Port 1, Lane 0)	2152	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.1.10b Tx Unit Interval, Max (Port 1, Lane 0)	1152	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.1.10b Tx Unit Interval, Max (Port 1, Lane 1)	2252	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.1.10b Tx Unit Interval, Max (Port 1, Lane 1)	1252	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.1.10b Tx Unit Interval, Max (Port 2, Lane 0)	2352	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.1.10b Tx Unit Interval, Max (Port 2, Lane 0)	1352	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.1.10b Tx Unit Interval, Max (Port 2, Lane 1)	2452	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.1.10b Tx Unit Interval, Max (Port 2, Lane 1)	1452	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.11 Tx SSC Down Spread Rate (Port 1, Lane 0)	2161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
1.1.11 Tx SSC Down Spread Rate (Port 1, Lane 0)	1161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
1.1.11 Tx SSC Down Spread Rate (Port 1, Lane 1)	2261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
1.1.11 Tx SSC Down Spread Rate (Port 1, Lane 1)	1261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
1.1.11 Tx SSC Down Spread Rate (Port 2, Lane 0)	2361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
1.1.11 Tx SSC Down Spread Rate (Port 2, Lane 0)	1361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
1.1.11 Tx SSC Down Spread Rate (Port 2, Lane 1)	2461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
1.1.11 Tx SSC Down Spread Rate (Port 2, Lane 1)	1461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
1.1.12 Tx SSC Down Spread Deviation (Port 1, Lane 0)	2162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
1.1.12 Tx SSC Down Spread Deviation (Port 1, Lane 0)	1162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
1.1.12 Tx SSC Down Spread Deviation (Port 1, Lane 1)	2262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
1.1.12 Tx SSC Down Spread Deviation (Port 1, Lane 1)	1262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
1.1.12 Tx SSC Down Spread Deviation (Port 2, Lane 0)	2362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.12 Tx SSC Down Spread Deviation (Port 2, Lane 0)	1362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
1.1.12 Tx SSC Down Spread Deviation (Port 2, Lane 1)	2462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
1.1.12 Tx SSC Down Spread Deviation (Port 2, Lane 1)	1462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
1.1.13 Tx SSC Phase Deviation (Port 1, Lane 0)	2171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
1.1.13 Tx SSC Phase Deviation (Port 1, Lane 0)	1171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
1.1.13 Tx SSC Phase Deviation (Port 1, Lane 1)	2271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
1.1.13 Tx SSC Phase Deviation (Port 1, Lane 1)	1271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
1.1.13 Tx SSC Phase Deviation (Port 2, Lane 0)	2371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
1.1.13 Tx SSC Phase Deviation (Port 2, Lane 0)	1371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
1.1.13 Tx SSC Phase Deviation (Port 2, Lane 1)	2471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
1.1.13 Tx SSC Phase Deviation (Port 2, Lane 1)	1471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
1.1.14 Tx SSC Phase Slew Rate (Port 1, Lane 0)	2172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
1.1.14 Tx SSC Phase Slew Rate (Port 1, Lane 0)	1172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.14 Tx SSC Phase Slew Rate (Port 1, Lane 1)	2272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
1.1.14 Tx SSC Phase Slew Rate (Port 1, Lane 1)	1272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
1.1.14 Tx SSC Phase Slew Rate (Port 2, Lane 0)	2372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
1.1.14 Tx SSC Phase Slew Rate (Port 2, Lane 0)	1372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
1.1.14 Tx SSC Phase Slew Rate (Port 2, Lane 1)	2472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
1.1.14 Tx SSC Phase Slew Rate (Port 2, Lane 1)	1472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
1.1.15 Tx AC Common Mode Voltage (Port 1, Lane 0)	2121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.1.15 Tx AC Common Mode Voltage (Port 1, Lane 0)	1121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.1.15 Tx AC Common Mode Voltage (Port 1, Lane 1)	2221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.1.15 Tx AC Common Mode Voltage (Port 1, Lane 1)	1221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.1.15 Tx AC Common Mode Voltage (Port 2, Lane 0)	2321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.1.15 Tx AC Common Mode Voltage (Port 2, Lane 0)	1321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.1.15 Tx AC Common Mode Voltage (Port 2, Lane 1)	2421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.1.15 Tx AC Common Mode Voltage (Port 2, Lane 1)	1421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.15.1 Tx Maximum Differential Voltage (Port 1, Lane 0)	2132	The maximum differential voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.1.15.1 Tx Maximum Differential Voltage (Port 1, Lane 0)	1132	The maximum differential voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.1.15.1 Tx Maximum Differential Voltage (Port 1, Lane 1)	2232	The maximum differential voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.1.15.1 Tx Maximum Differential Voltage (Port 1, Lane 1)	1232	The maximum differential voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.1.15.1 Tx Maximum Differential Voltage (Port 2, Lane 0)	2332	The maximum differential voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.1.15.1 Tx Maximum Differential Voltage (Port 2, Lane 0)	1332	The maximum differential voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.1.15.1 Tx Maximum Differential Voltage (Port 2, Lane 1)	2432	The maximum differential voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.1.15.1 Tx Maximum Differential Voltage (Port 2, Lane 1)	1432	The maximum differential voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.1.16 Tx Eye Diagram (Port 1, Lane 0)	2131	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
1.1.16 Tx Eye Diagram (Port 1, Lane 0)	1131	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
1.1.16 Tx Eye Diagram (Port 1, Lane 1)	2231	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
1.1.16 Tx Eye Diagram (Port 1, Lane 1)	1231	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
1.1.16 Tx Eye Diagram (Port 2, Lane 0)	2331	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
1.1.16 Tx Eye Diagram (Port 2, Lane 0)	1331	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.16 Tx Eye Diagram (Port 2, Lane 1)	2431	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
1.1.16 Tx Eye Diagram (Port 2, Lane 1)	1431	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
1.1.16 Tx Platform Equalization (Port 1, Lane 0)	2181	The platform equalization level (PLATFORM_EQ) at TP1 of a Thunderbolt device must be within the specification.
1.1.16 Tx Platform Equalization (Port 1, Lane 0)	1181	The platform equalization level (PLATFORM_EQ) at TP1 of a Thunderbolt host must be within the specification.
1.1.16 Tx Platform Equalization (Port 1, Lane 1)	2281	The platform equalization level (PLATFORM_EQ) at TP1 of a Thunderbolt device must be within the specification.
1.1.16 Tx Platform Equalization (Port 1, Lane 1)	1281	The platform equalization level (PLATFORM_EQ) at TP1 of a Thunderbolt host must be within the specification.
1.1.16 Tx Platform Equalization (Port 2, Lane 0)	2381	The platform equalization level (PLATFORM_EQ) at TP1 of a Thunderbolt device must be within the specification.
1.1.16 Tx Platform Equalization (Port 2, Lane 0)	1381	The platform equalization level (PLATFORM_EQ) at TP1 of a Thunderbolt host must be within the specification.
1.1.16 Tx Platform Equalization (Port 2, Lane 1)	2481	The platform equalization level (PLATFORM_EQ) at TP1 of a Thunderbolt device must be within the specification.
1.1.16 Tx Platform Equalization (Port 2, Lane 1)	1481	The platform equalization level (PLATFORM_EQ) at TP1 of a Thunderbolt host must be within the specification.
1.1.17 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	2991	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
1.1.17 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	1991	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
1.1.17 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	2992	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
1.1.17 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	1992	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
1.1.17 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	2993	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.17 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	1993	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
1.1.17 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	2994	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
1.1.17 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	1994	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
1.1.18 Tx Equalization Preshoot (Port 2, Lane 1)	1540	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.18 Tx Equalization Preshoot (Port 2, Lane 1)	2540	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.18 Tx Equalization Preshoot(Port 1, Lane 0)	1510	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.18 Tx Equalization Preshoot(Port 1, Lane 0)	2510	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.18 Tx Equalization Preshoot(Port 1, Lane 1)	1520	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.18 Tx Equalization Preshoot(Port 1, Lane 1)	2520	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.18 Tx Equalization Preshoot(Port 2, Lane 0)	1530	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.18 Tx Equalization Preshoot(Port 2, Lane 0)	2530	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.19 Tx Equalization Deemphasis(Port 1, Lane 0)	1610	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.19 Tx Equalization Deemphasis(Port 1, Lane 0)	2610	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.19 Tx Equalization Deemphasis(Port 1, Lane 1)	1620	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.19 Tx Equalization Deemphasis(Port 1, Lane 1)	2620	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.19 Tx Equalization Deemphasis(Port 2, Lane 0)	1630	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.19 Tx Equalization Deemphasis(Port 2, Lane 0)	2630	The equalization level at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.19 Tx Equalization Deemphasis(Port 2, Lane 1)	1640	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.19 Tx Equalization Deemphasis(Port 2, Lane 1)	2640	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.1.2 Tx Fall Time (Port 1, Lane 0)	2112	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.2 Tx Fall Time (Port 1, Lane 0)	1112	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.2 Tx Fall Time (Port 1, Lane 1)	2212	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.2 Tx Fall Time (Port 1, Lane 1)	1212	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.2 Tx Fall Time (Port 2, Lane 0)	2312	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.2 Tx Fall Time (Port 2, Lane 0)	1312	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.2 Tx Fall Time (Port 2, Lane 1)	2412	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.2 Tx Fall Time (Port 2, Lane 1)	1412	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.1.20 Tx Swing Preset 15 (Port 1, Lane 0)	2710	The Tx Swing Preset 15 of a Thunderbolt Device must be within the specification.
1.1.20 Tx Swing Preset 15 (Port 1, Lane 0)	1710	The Tx Swing Preset 15 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.20 Tx Swing Preset 15 (Port 1, Lane 1)	2720	The Tx Swing Preset 15 of a Thunderbolt Device must be within the specification.
1.1.20 Tx Swing Preset 15 (Port 1, Lane 1)	1720	The Tx Swing Preset 15 of a Thunderbolt host must be within the specification.
1.1.20 Tx Swing Preset 15 (Port 2, Lane 0)	2730	The Tx Swing Preset 15 of a Thunderbolt Device must be within the specification.
1.1.20 Tx Swing Preset 15 (Port 2, Lane 0)	1730	The Tx Swing Preset 15 of a Thunderbolt host must be within the specification.
1.1.20 Tx Swing Preset 15 (Port 2, Lane 1)	2740	The Tx Swing Preset 15 of a Thunderbolt Device must be within the specification.
1.1.20 Tx Swing Preset 15 (Port 2, Lane 1)	1740	The Tx Swing Preset 15 of a Thunderbolt host must be within the specification.
1.1.3 Tx Sum of Uncorrelated Jitter (Port 1, Lane 0)	1871	The sum of uncorrelated jitter (UJ) of a Thunderbolt host must be less than maximum limit.
1.1.3 Tx Sum of Uncorrelated Jitter (Port 1, Lane 1)	1872	The sum of uncorrelated jitter (UJ) of a Thunderbolt host must be less than maximum limit.
1.1.3 Tx Sum of Uncorrelated Jitter (Port 2, Lane 0)	1873	The sum of uncorrelated jitter (UJ) of a Thunderbolt host must be less than maximum limit.
1.1.3 Tx Sum of Uncorrelated Jitter (Port 2, Lane 1)	1874	The sum of uncorrelated jitter (UJ) of a Thunderbolt host must be less than maximum limit.
1.1.4 Tx Sum of Uncorrelated Deterministic Jitter (Port 1, Lane 0)	1971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
1.1.4 Tx Sum of Uncorrelated Deterministic Jitter (Port 1, Lane 1)	1972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
1.1.4 Tx Sum of Uncorrelated Deterministic Jitter (Port 2, Lane 0)	1973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
1.1.4 Tx Sum of Uncorrelated Deterministic Jitter (Port 2, Lane 1)	1974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
1.1.4 Tx Sum of Uncorrelated Jitter (Port 1, Lane 0)	2871	The sum of uncorrelated jitter (UJ) of a Thunderbolt device must be less than maximum limit.
1.1.4 Tx Sum of Uncorrelated Jitter (Port 1, Lane 1)	2872	The sum of uncorrelated jitter (UJ) of a Thunderbolt device must be less than maximum limit.
1.1.4 Tx Sum of Uncorrelated Jitter (Port 2, Lane 0)	2873	The sum of uncorrelated jitter (UJ) of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.4 Tx Sum of Uncorrelated Jitter (Port 2, Lane 1)	2874	The sum of uncorrelated jitter (UJ) of a Thunderbolt device must be less than maximum limit.
1.1.4 Tx Total Jitter, CDR1 (Port 1, Lane 0)	2141	The total jitter (TJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.4 Tx Total Jitter, CDR1 (Port 1, Lane 0)	1141	The total jitter (TJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.4 Tx Total Jitter, CDR1 (Port 1, Lane 1)	2241	The total jitter (TJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.4 Tx Total Jitter, CDR1 (Port 1, Lane 1)	1241	The total jitter (TJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.4 Tx Total Jitter, CDR1 (Port 2, Lane 0)	2341	The total jitter (TJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.4 Tx Total Jitter, CDR1 (Port 2, Lane 0)	1341	The total jitter (TJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.4 Tx Total Jitter, CDR1 (Port 2, Lane 1)	2441	The total jitter (TJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.4 Tx Total Jitter, CDR1 (Port 2, Lane 1)	1441	The total jitter (TJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.4.1 Tx Random Jitter, CDR1 (Port 1, Lane 0)	2142	The random jitter (RJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.4.1 Tx Random Jitter, CDR1 (Port 1, Lane 0)	1142	The random jitter (RJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.4.1 Tx Random Jitter, CDR1 (Port 1, Lane 1)	2242	The random jitter (RJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.4.1 Tx Random Jitter, CDR1 (Port 1, Lane 1)	1242	The random jitter (RJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.4.1 Tx Random Jitter, CDR1 (Port 2, Lane 0)	2342	The random jitter (RJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.4.1 Tx Random Jitter, CDR1 (Port 2, Lane 0)	1342	The random jitter (RJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.4.1 Tx Random Jitter, CDR1 (Port 2, Lane 1)	2442	The random jitter (RJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.4.1 Tx Random Jitter, CDR1 (Port 2, Lane 1)	1442	The random jitter (RJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.5 Tx Sum of Uncorrelated Deterministic Jitter (Port 1, Lane 0)	2971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.5 Tx Sum of Uncorrelated Deterministic Jitter (Port 1, Lane 1)	2972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
1.1.5 Tx Sum of Uncorrelated Deterministic Jitter (Port 2, Lane 0)	2973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
1.1.5 Tx Sum of Uncorrelated Deterministic Jitter (Port 2, Lane 1)	2974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
1.1.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	2771	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	1771	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	2772	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	1772	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	2773	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	1773	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	2774	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	1774	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.5 Tx Total Jitter (Port 1, Lane 0)	10671	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
1.1.5 Tx Total Jitter (Port 1, Lane 1)	10672	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
1.1.5 Tx Total Jitter (Port 2, Lane 0)	10673	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
1.1.5 Tx Total Jitter (Port 2, Lane 1)	10674	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
1.1.5 Tx Total Jitter, CDR2 (Port 1, Lane 0)	2143	The total jitter (TJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.5 Tx Total Jitter, CDR2 (Port 1, Lane 0)	1143	The total jitter (TJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.5 Tx Total Jitter, CDR2 (Port 1, Lane 1)	2243	The total jitter (TJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.5 Tx Total Jitter, CDR2 (Port 1, Lane 1)	1243	The total jitter (TJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.5 Tx Total Jitter, CDR2 (Port 2, Lane 0)	2343	The total jitter (TJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.5 Tx Total Jitter, CDR2 (Port 2, Lane 0)	1343	The total jitter (TJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.5 Tx Total Jitter, CDR2 (Port 2, Lane 1)	2443	The total jitter (TJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.
1.1.5 Tx Total Jitter, CDR2 (Port 2, Lane 1)	1443	The total jitter (TJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25. Total jitter is the sum of all DJ plus 14.7 times the RJ rms.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.5.1 Tx Random Jitter, CDR2 (Port 1, Lane 0)	2144	The random jitter (RJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25.
1.1.5.1 Tx Random Jitter, CDR2 (Port 1, Lane 0)	1144	The random jitter (RJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25.
1.1.5.1 Tx Random Jitter, CDR2 (Port 1, Lane 1)	2244	The random jitter (RJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25.
1.1.5.1 Tx Random Jitter, CDR2 (Port 1, Lane 1)	1244	The random jitter (RJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25.
1.1.5.1 Tx Random Jitter, CDR2 (Port 2, Lane 0)	2344	The random jitter (RJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25.
1.1.5.1 Tx Random Jitter, CDR2 (Port 2, Lane 0)	1344	The random jitter (RJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25.
1.1.5.1 Tx Random Jitter, CDR2 (Port 2, Lane 1)	2444	The random jitter (RJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25.
1.1.5.1 Tx Random Jitter, CDR2 (Port 2, Lane 1)	1444	The random jitter (RJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR2 with closed loop corner frequency 5MHz and damping factor 1.25.
1.1.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	2881	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	1881	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	2882	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	1882	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	2883	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	1883	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	2884	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	1884	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.6a Tx Low-Frequency Total Jitter (Port 1, Lane 0)	2145	The Low-Frequency Total Jitter (TJ_LF) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6a Tx Low-Frequency Total Jitter (Port 1, Lane 0)	1145	The Low-Frequency Total Jitter (TJ_LF) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6a Tx Low-Frequency Total Jitter (Port 1, Lane 1)	2245	The Low-Frequency Total Jitter (TJ_LF) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6a Tx Low-Frequency Total Jitter (Port 1, Lane 1)	1245	The Low-Frequency Total Jitter (TJ_LF) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6a Tx Low-Frequency Total Jitter (Port 2, Lane 0)	2345	The Low-Frequency Total Jitter (TJ_LF) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6a Tx Low-Frequency Total Jitter (Port 2, Lane 0)	1345	The Low-Frequency Total Jitter (TJ_LF) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.6a Tx Low-Frequency Total Jitter (Port 2, Lane 1)	2445	The Low-Frequency Total Jitter (TJ_LF) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6a Tx Low-Frequency Total Jitter (Port 2, Lane 1)	1445	The Low-Frequency Total Jitter (TJ_LF) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6b Tx Low-Frequency Deterministic Jitter (Port 1, Lane 0)	2148	The Low-Frequency Deterministic Jitter (DJ_LF) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6b Tx Low-Frequency Deterministic Jitter (Port 1, Lane 0)	1148	The Low-Frequency Deterministic Jitter (DJ_LF) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6b Tx Low-Frequency Deterministic Jitter (Port 1, Lane 1)	2248	The Low-Frequency Deterministic Jitter (DJ_LF) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6b Tx Low-Frequency Deterministic Jitter (Port 1, Lane 1)	1248	The Low-Frequency Deterministic Jitter (DJ_LF) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6b Tx Low-Frequency Deterministic Jitter (Port 2, Lane 0)	2348	The Low-Frequency Deterministic Jitter (DJ_LF) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6b Tx Low-Frequency Deterministic Jitter (Port 2, Lane 0)	1348	The Low-Frequency Deterministic Jitter (DJ_LF) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6b Tx Low-Frequency Deterministic Jitter (Port 2, Lane 1)	2448	The Low-Frequency Deterministic Jitter (DJ_LF) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.
1.1.6b Tx Low-Frequency Deterministic Jitter (Port 2, Lane 1)	1448	The Low-Frequency Deterministic Jitter (DJ_LF) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured with CDR1 and 1st order LPF with 3dB point 11MHz.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.7 Tx Data Dependent Jitter (Port 1, Lane 0)	2146	The data dependant jitter (DDJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.7 Tx Data Dependent Jitter (Port 1, Lane 0)	1146	The data dependant jitter (DDJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.7 Tx Data Dependent Jitter (Port 1, Lane 1)	2246	The data dependant jitter (DDJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.7 Tx Data Dependent Jitter (Port 1, Lane 1)	1246	The data dependant jitter (DDJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.7 Tx Data Dependent Jitter (Port 2, Lane 0)	2346	The data dependant jitter (DDJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.7 Tx Data Dependent Jitter (Port 2, Lane 0)	1346	The data dependant jitter (DDJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.7 Tx Data Dependent Jitter (Port 2, Lane 1)	2446	The data dependant jitter (DDJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.7 Tx Data Dependent Jitter (Port 2, Lane 1)	1446	The data dependant jitter (DDJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.7 Tx Total Jitter (Port 1, Lane 0)	2671	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.7 Tx Total Jitter (Port 1, Lane 0)	1671	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
1.1.7 Tx Total Jitter (Port 1, Lane 1)	2672	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
1.1.7 Tx Total Jitter (Port 1, Lane 1)	1672	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
1.1.7 Tx Total Jitter (Port 2, Lane 0)	2673	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
1.1.7 Tx Total Jitter (Port 2, Lane 0)	1673	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
1.1.7 Tx Total Jitter (Port 2, Lane 1)	2674	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
1.1.7 Tx Total Jitter (Port 2, Lane 1)	1674	The total jitter (TJ) of a Thunderbolt host must be less than maximum limit.
1.1.8 Tx Sum of Uncorrelated Deterministic Jitter and Random Jitter (Port 1, Lane 0)	2147	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.8 Tx Sum of Uncorrelated Deterministic Jitter and Random Jitter (Port 1, Lane 0)	1147	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.8 Tx Sum of Uncorrelated Deterministic Jitter and Random Jitter (Port 1, Lane 1)	2247	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.8 Tx Sum of Uncorrelated Deterministic Jitter and Random Jitter (Port 1, Lane 1)	1247	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.8 Tx Sum of Uncorrelated Deterministic Jitter and Random Jitter (Port 2, Lane 0)	2347	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.8 Tx Sum of Uncorrelated Deterministic Jitter and Random Jitter (Port 2, Lane 0)	1347	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.8 Tx Sum of Uncorrelated Deterministic Jitter and Random Jitter (Port 2, Lane 1)	2447	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP1 of a Thunderbolt device must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.8 Tx Sum of Uncorrelated Deterministic Jitter and Random Jitter (Port 2, Lane 1)	1447	The sum of uncorrelated deterministic jitter and random jitter (UJ) at TP1 of a Thunderbolt host must be less than maximum limit. The jitter will be measured using 2nd order CDR1 with closed loop corner frequency 5MHz and damping factor 0.58.
1.1.8 Tx Total Jitter TP3EQ (Port 1, Lane 0)	2661	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.8 Tx Total Jitter TP3EQ (Port 1, Lane 0)	1661	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.8 Tx Total Jitter TP3EQ (Port 1, Lane 1)	2662	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.8 Tx Total Jitter TP3EQ (Port 1, Lane 1)	1662	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.8 Tx Total Jitter TP3EQ (Port 2, Lane 0)	2663	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.8 Tx Total Jitter TP3EQ (Port 2, Lane 0)	1663	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.8 Tx Total Jitter TP3EQ (Port 2, Lane 1)	2664	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.1.8 Tx Total Jitter TP3EQ (Port 2, Lane 1)	1664	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.1.9a Tx Unit Interval Mean, Min (Port 1, Lane 0)	2153	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9a Tx Unit Interval Mean, Min (Port 1, Lane 0)	1153	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.9a Tx Unit Interval Mean, Min (Port 1, Lane 1)	2253	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9a Tx Unit Interval Mean, Min (Port 1, Lane 1)	1253	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9a Tx Unit Interval Mean, Min (Port 2, Lane 0)	2353	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9a Tx Unit Interval Mean, Min (Port 2, Lane 0)	1353	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9a Tx Unit Interval Mean, Min (Port 2, Lane 1)	2453	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9a Tx Unit Interval Mean, Min (Port 2, Lane 1)	1453	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9b Tx Unit Interval Mean, Max (Port 1, Lane 0)	2154	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9b Tx Unit Interval Mean, Max (Port 1, Lane 0)	1154	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9b Tx Unit Interval Mean, Max (Port 1, Lane 1)	2254	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9b Tx Unit Interval Mean, Max (Port 1, Lane 1)	1254	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.1.9b Tx Unit Interval Mean, Max (Port 2, Lane 0)	2354	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9b Tx Unit Interval Mean, Max (Port 2, Lane 0)	1354	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9b Tx Unit Interval Mean, Max (Port 2, Lane 1)	2454	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.1.9b Tx Unit Interval Mean, Max (Port 2, Lane 1)	1454	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.0a Preset Calibration (Port 1, Lane 0)	20810	The Preset Calibration is used to find the optimized preset for the platform.
1.2.0a Preset Calibration (Port 1, Lane 1)	20811	The Preset Calibration is used to find the optimized preset for the platform.
1.2.0a Preset Calibration (Port 1, Lane 1)	20813	The Preset Calibration is used to find the optimized preset for the platform.
1.2.0a Preset Calibration (Port 2, Lane 0)	20812	The Preset Calibration is used to find the optimized preset for the platform.
1.2.0b CTLE Calibration (Port 1, Lane 0)	20820	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.2.0b CTLE Calibration (Port 1, Lane 1)	20821	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.2.0b CTLE Calibration (Port 2, Lane 0)	20822	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.2.0b CTLE Calibration (Port 2, Lane 1)	20823	The CTLE Calibration is used to find the optimized DC gain value for the platform.
1.2.1 Tx Rise Time (Port 1, Lane 0)	20111	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.1 Tx Rise Time (Port 1, Lane 0)	10111	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.1 Tx Rise Time (Port 1, Lane 1)	20211	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.1 Tx Rise Time (Port 1, Lane 1)	10211	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.1 Tx Rise Time (Port 2, Lane 0)	20311	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.1 Tx Rise Time (Port 2, Lane 0)	10311	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.1 Tx Rise Time (Port 2, Lane 1)	20411	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.1 Tx Rise Time (Port 2, Lane 1)	10411	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.10a Tx Unit Interval, Min (Port 1, Lane 0)	20151	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.2.10a Tx Unit Interval, Min (Port 1, Lane 0)	10151	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.2.10a Tx Unit Interval, Min (Port 1, Lane 1)	20251	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.2.10a Tx Unit Interval, Min (Port 1, Lane 1)	10251	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.2.10a Tx Unit Interval, Min (Port 2, Lane 0)	20351	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.2.10a Tx Unit Interval, Min (Port 2, Lane 0)	10351	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.2.10a Tx Unit Interval, Min (Port 2, Lane 1)	20451	The minimum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.2.10a Tx Unit Interval, Min (Port 2, Lane 1)	10451	The minimum unit interval at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.10b Tx Unit Interval, Max (Port 1, Lane 0)	20152	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.2.10b Tx Unit Interval, Max (Port 1, Lane 0)	10152	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.2.10b Tx Unit Interval, Max (Port 1, Lane 1)	20252	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.2.10b Tx Unit Interval, Max (Port 1, Lane 1)	10252	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.2.10b Tx Unit Interval, Max (Port 2, Lane 0)	20352	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.2.10b Tx Unit Interval, Max (Port 2, Lane 0)	10352	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.2.10b Tx Unit Interval, Max (Port 2, Lane 1)	20452	The maximum unit interval at TP1 of a Thunderbolt device must be within the specification.
1.2.10b Tx Unit Interval, Max (Port 2, Lane 1)	10452	The maximum unit interval at TP1 of a Thunderbolt host must be within the specification.
1.2.11 Tx SSC Down Spread Rate (Port 1, Lane 0)	20161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
1.2.11 Tx SSC Down Spread Rate (Port 1, Lane 0)	10161	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
1.2.11 Tx SSC Down Spread Rate (Port 1, Lane 1)	20261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
1.2.11 Tx SSC Down Spread Rate (Port 1, Lane 1)	10261	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
1.2.11 Tx SSC Down Spread Rate (Port 2, Lane 0)	20361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.
1.2.11 Tx SSC Down Spread Rate (Port 2, Lane 0)	10361	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
1.2.11 Tx SSC Down Spread Rate (Port 2, Lane 1)	20461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.11 Tx SSC Down Spread Rate (Port 2, Lane 1)	10461	The spread spectrum clocking (SSC) modulation frequency at TP1 of a Thunderbolt host must be within the specification.
1.2.12 Tx SSC Down Spread Deviation (Port 1, Lane 0)	20162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
1.2.12 Tx SSC Down Spread Deviation (Port 1, Lane 0)	10162	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
1.2.12 Tx SSC Down Spread Deviation (Port 1, Lane 1)	20262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
1.2.12 Tx SSC Down Spread Deviation (Port 1, Lane 1)	10262	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
1.2.12 Tx SSC Down Spread Deviation (Port 2, Lane 0)	20362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
1.2.12 Tx SSC Down Spread Deviation (Port 2, Lane 0)	10362	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
1.2.12 Tx SSC Down Spread Deviation (Port 2, Lane 1)	20462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt device must be within the specification.
1.2.12 Tx SSC Down Spread Deviation (Port 2, Lane 1)	10462	The spread spectrum clocking (SSC) modulation deviation at TP1 of a Thunderbolt host must be within the specification.
1.2.13 Tx SSC Phase Deviation (Port 1, Lane 0)	20171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
1.2.13 Tx SSC Phase Deviation (Port 1, Lane 0)	10171	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
1.2.13 Tx SSC Phase Deviation (Port 1, Lane 1)	20271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
1.2.13 Tx SSC Phase Deviation (Port 1, Lane 1)	10271	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.13 Tx SSC Phase Deviation (Port 2, Lane 0)	20371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
1.2.13 Tx SSC Phase Deviation (Port 2, Lane 0)	10371	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
1.2.13 Tx SSC Phase Deviation (Port 2, Lane 1)	20471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt device must be within the specification.
1.2.13 Tx SSC Phase Deviation (Port 2, Lane 1)	10471	The spread spectrum clocking (SSC) phase jitter at TP1 of a Thunderbolt host must be within the specification.
1.2.14 Tx SSC Phase Slew Rate (Port 1, Lane 0)	20172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
1.2.14 Tx SSC Phase Slew Rate (Port 1, Lane 0)	10172	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
1.2.14 Tx SSC Phase Slew Rate (Port 1, Lane 1)	20272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
1.2.14 Tx SSC Phase Slew Rate (Port 1, Lane 1)	10272	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
1.2.14 Tx SSC Phase Slew Rate (Port 2, Lane 0)	20372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
1.2.14 Tx SSC Phase Slew Rate (Port 2, Lane 0)	10372	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
1.2.14 Tx SSC Phase Slew Rate (Port 2, Lane 1)	20472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt device must be within the specification.
1.2.14 Tx SSC Phase Slew Rate (Port 2, Lane 1)	10472	The spread spectrum clocking (SSC) phase slew rate at TP1 of a Thunderbolt host must be within the specification.
1.2.15 Tx AC Common Mode Voltage (Port 1, Lane 0)	20121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.15 Tx AC Common Mode Voltage (Port 1, Lane 0)	10121	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.2.15 Tx AC Common Mode Voltage (Port 1, Lane 1)	20221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.2.15 Tx AC Common Mode Voltage (Port 1, Lane 1)	10221	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.2.15 Tx AC Common Mode Voltage (Port 2, Lane 0)	20321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.2.15 Tx AC Common Mode Voltage (Port 2, Lane 0)	10321	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.2.15 Tx AC Common Mode Voltage (Port 2, Lane 1)	20421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt device must be less than maximum limit.
1.2.15 Tx AC Common Mode Voltage (Port 2, Lane 1)	10421	The AC common mode peak-to-peak voltage at TP1 of a Thunderbolt host must be less than maximum limit.
1.2.16 Tx Eye Diagram (Port 1, Lane 0)	20131	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
1.2.16 Tx Eye Diagram (Port 1, Lane 0)	10131	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
1.2.16 Tx Eye Diagram (Port 1, Lane 1)	20231	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
1.2.16 Tx Eye Diagram (Port 1, Lane 1)	10231	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
1.2.16 Tx Eye Diagram (Port 2, Lane 0)	20331	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
1.2.16 Tx Eye Diagram (Port 2, Lane 0)	10331	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.
1.2.16 Tx Eye Diagram (Port 2, Lane 1)	20431	The eye diagram at TP1 of a Thunderbolt device must be within the template as described in the specification.
1.2.16 Tx Eye Diagram (Port 2, Lane 1)	10431	The eye diagram at TP1 of a Thunderbolt host must be within the template as described in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.17 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	20991	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
1.2.17 Tx Eye Diagram TP3EQ (Port 1, Lane 0)	10991	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
1.2.17 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	20992	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
1.2.17 Tx Eye Diagram TP3EQ (Port 1, Lane 1)	10992	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
1.2.17 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	20993	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
1.2.17 Tx Eye Diagram TP3EQ (Port 2, Lane 0)	10993	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
1.2.17 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	20994	The eye diagram at TP3EQ of a Thunderbolt device must be within the template as described in the specification.
1.2.17 Tx Eye Diagram TP3EQ (Port 2, Lane 1)	10994	The eye diagram at TP3EQ of a Thunderbolt host must be within the template as described in the specification.
1.2.18 Tx Equalization Preshoot (Port 2, Lane 1)	10540	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.18 Tx Equalization Preshoot (Port 2, Lane 1)	20540	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.18 Tx Equalization Preshoot(Port 1, Lane 0)	10510	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.18 Tx Equalization Preshoot(Port 1, Lane 0)	20510	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.18 Tx Equalization Preshoot(Port 1, Lane 1)	10520	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.18 Tx Equalization Preshoot(Port 1, Lane 1)	20520	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.18 Tx Equalization Preshoot(Port 2, Lane 0)	10530	The equalization level at TP1 of a Thunderbolt device must be within the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.18 Tx Equalization Preshoot(Port 2, Lane 0)	20530	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.19 Tx Equalization Deemphasis(Port 1, Lane 0)	10610	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.19 Tx Equalization Deemphasis(Port 1, Lane 0)	20610	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.19 Tx Equalization Deemphasis(Port 1, Lane 1)	10620	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.19 Tx Equalization Deemphasis(Port 1, Lane 1)	20620	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.19 Tx Equalization Deemphasis(Port 2, Lane 0)	10630	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.19 Tx Equalization Deemphasis(Port 2, Lane 0)	20630	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.19 Tx Equalization Deemphasis(Port 2, Lane 1)	10640	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.19 Tx Equalization Deemphasis(Port 2, Lane 1)	20640	The equalization level at TP1 of a Thunderbolt device must be within the specification.
1.2.2 Tx Fall Time (Port 1, Lane 0)	20112	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.2 Tx Fall Time (Port 1, Lane 0)	10112	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.2 Tx Fall Time (Port 1, Lane 1)	20212	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.2 Tx Fall Time (Port 1, Lane 1)	10212	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.2 Tx Fall Time (Port 2, Lane 0)	20312	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.2 Tx Fall Time (Port 2, Lane 0)	10312	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.2 Tx Fall Time (Port 2, Lane 1)	20412	The Tx output rise time and fall time at TP1 of a Thunderbolt device must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.2 Tx Fall Time (Port 2, Lane 1)	10412	The Tx output rise time and fall time at TP1 of a Thunderbolt host must be greater than minimum limit. The rise/fall time measurement is based on the 20% to 80% of the Vpp of the signal.
1.2.20 Tx Swing Preset 15 (Port 1, Lane 0)	20710	The Tx Swing Preset 15 of a Thunderbolt Device must be within the specification.
1.2.20 Tx Swing Preset 15 (Port 1, Lane 0)	10710	The Tx Swing Preset 15 of a Thunderbolt host must be within the specification.
1.2.20 Tx Swing Preset 15 (Port 1, Lane 1)	20720	The Tx Swing Preset 15 of a Thunderbolt Device must be within the specification.
1.2.20 Tx Swing Preset 15 (Port 1, Lane 1)	10720	The Tx Swing Preset 15 of a Thunderbolt host must be within the specification.
1.2.20 Tx Swing Preset 15 (Port 2, Lane 0)	20730	The Tx Swing Preset 15 of a Thunderbolt Device must be within the specification.
1.2.20 Tx Swing Preset 15 (Port 2, Lane 0)	10730	The Tx Swing Preset 15 of a Thunderbolt host must be within the specification.
1.2.20 Tx Swing Preset 15 (Port 2, Lane 1)	20740	The Tx Swing Preset 15 of a Thunderbolt Device must be within the specification.
1.2.20 Tx Swing Preset 15 (Port 2, Lane 1)	10740	The Tx Swing Preset 15 of a Thunderbolt host must be within the specification.
1.2.3 Tx Sum of Uncorrelated Jitter (Port 1, Lane 0)	10871	The sum of uncorrelated jitter (UJ) of a Thunderbolt host must be less than maximum limit.
1.2.3 Tx Sum of Uncorrelated Jitter (Port 1, Lane 1)	10872	The sum of uncorrelated jitter (UJ) of a Thunderbolt host must be less than maximum limit.
1.2.3 Tx Sum of Uncorrelated Jitter (Port 2, Lane 0)	10873	The sum of uncorrelated jitter (UJ) of a Thunderbolt host must be less than maximum limit.
1.2.3 Tx Sum of Uncorrelated Jitter (Port 2, Lane 1)	10874	The sum of uncorrelated jitter (UJ) of a Thunderbolt host must be less than maximum limit.
1.2.4 Tx Sum of Uncorrelated Deterministic Jitter (Port 1, Lane 0)	10971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.4 Tx Sum of Uncorrelated Deterministic Jitter (Port 1, Lane 1)	10972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
1.2.4 Tx Sum of Uncorrelated Deterministic Jitter (Port 2, Lane 0)	10973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
1.2.4 Tx Sum of Uncorrelated Deterministic Jitter (Port 2, Lane 1)	10974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt host must be less than the maximum limit.
1.2.4 Tx Sum of Uncorrelated Jitter (Port 1, Lane 0)	20871	The sum of uncorrelated jitter (UJ) of a Thunderbolt device must be less than maximum limit.
1.2.4 Tx Sum of Uncorrelated Jitter (Port 1, Lane 1)	20872	The sum of uncorrelated jitter (UJ) of a Thunderbolt device must be less than maximum limit.
1.2.4 Tx Sum of Uncorrelated Jitter (Port 2, Lane 0)	20873	The sum of uncorrelated jitter (UJ) of a Thunderbolt device must be less than maximum limit.
1.2.4 Tx Sum of Uncorrelated Jitter (Port 2, Lane 1)	20874	The sum of uncorrelated jitter (UJ) of a Thunderbolt device must be less than maximum limit.
1.2.5 Tx Sum of Uncorrelated Deterministic Jitter (Port 1, Lane 0)	20971	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
1.2.5 Tx Sum of Uncorrelated Deterministic Jitter (Port 1, Lane 1)	20972	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
1.2.5 Tx Sum of Uncorrelated Deterministic Jitter (Port 2, Lane 0)	20973	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
1.2.5 Tx Sum of Uncorrelated Deterministic Jitter (Port 2, Lane 1)	20974	The sum of uncorrelated deterministic jitter (UDJ) of a Thunderbolt device must be less than the maximum limit.
1.2.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	20771	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 1, Lane 0)	10771	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	20772	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 1, Lane 1)	10772	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	20773	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 2, Lane 0)	10773	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	20774	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.5 Tx Sum of Uncorrelated Jitter TP3EQ (Port 2, Lane 1)	10774	The sum of uncorrelated jitter (UJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	20881	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 0)	10881	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	20882	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 1, Lane 1)	10882	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	20883	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 0)	10883	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	20884	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.6 Tx Sum of Uncorrelated Deterministic Jitter TP3EQ (Port 2, Lane 1)	10884	The sum of uncorrelated deterministic jitter (UDJ)at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.7 Tx Total Jitter (Port 1, Lane 0)	20671	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
1.2.7 Tx Total Jitter (Port 1, Lane 1)	20672	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
1.2.7 Tx Total Jitter (Port 2, Lane 0)	20673	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.
1.2.7 Tx Total Jitter (Port 2, Lane 1)	20674	The total jitter (TJ) of a Thunderbolt device must be less than maximum limit.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.8 Tx Total Jitter TP3EQ (Port 1, Lane 0)	20661	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.8 Tx Total Jitter TP3EQ (Port 1, Lane 0)	10661	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.8 Tx Total Jitter TP3EQ (Port 1, Lane 1)	20662	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.8 Tx Total Jitter TP3EQ (Port 1, Lane 1)	10662	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.8 Tx Total Jitter TP3EQ (Port 2, Lane 0)	20663	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.8 Tx Total Jitter TP3EQ (Port 2, Lane 0)	10663	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.8 Tx Total Jitter TP3EQ (Port 2, Lane 1)	20664	The total jitter (TJ) at TP3EQ of a Thunderbolt device must be less than maximum limit.
1.2.8 Tx Total Jitter TP3EQ (Port 2, Lane 1)	10664	The total jitter (TJ) at TP3EQ of a Thunderbolt host must be less than maximum limit.
1.2.9a Tx Unit Interval Mean, Min (Port 1, Lane 0)	20153	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9a Tx Unit Interval Mean, Min (Port 1, Lane 0)	10153	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9a Tx Unit Interval Mean, Min (Port 1, Lane 1)	20253	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9a Tx Unit Interval Mean, Min (Port 1, Lane 1)	10253	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9a Tx Unit Interval Mean, Min (Port 2, Lane 0)	20353	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9a Tx Unit Interval Mean, Min (Port 2, Lane 0)	10353	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1.2.9a Tx Unit Interval Mean, Min (Port 2, Lane 1)	20453	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9a Tx Unit Interval Mean, Min (Port 2, Lane 1)	10453	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9b Tx Unit Interval Mean, Max (Port 1, Lane 0)	20154	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9b Tx Unit Interval Mean, Max (Port 1, Lane 0)	10154	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9b Tx Unit Interval Mean, Max (Port 1, Lane 1)	20254	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9b Tx Unit Interval Mean, Max (Port 1, Lane 1)	10254	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9b Tx Unit Interval Mean, Max (Port 2, Lane 0)	20354	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9b Tx Unit Interval Mean, Max (Port 2, Lane 0)	10354	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9b Tx Unit Interval Mean, Max (Port 2, Lane 1)	20454	The mean unit interval at TP1 of a Thunderbolt device must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
1.2.9b Tx Unit Interval Mean, Max (Port 2, Lane 1)	10454	The mean unit interval at TP1 of a Thunderbolt host must be within the specification. The average UI should measured over windows at the size of one SSC cycle.
CTLE Calibration (Port 1, Lane 0)	10820	The CTLE Calibration is used to find the optimized DC gain value for the platform.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
CTLE Calibration (Port 1, Lane 1)	10821	The CTLE Calibration is used to find the optimized DC gain value for the platform.
CTLE Calibration (Port 1, Lane 1)	10823	The CTLE Calibration is used to find the optimized DC gain value for the platform.
CTLE Calibration (Port 2, Lane 0)	10822	The CTLE Calibration is used to find the optimized DC gain value for the platform.
Preset Calibration (Port 1, Lane 0)	10810	The Preset Calibration is used to find the optimized preset for the platform.
Preset Calibration (Port 1, Lane 1)	10811	The Preset Calibration is used to find the optimized preset for the platform.
Preset Calibration (Port 2, Lane 0)	10812	The Preset Calibration is used to find the optimized preset for the platform.
Preset Calibration (Port 2, Lane 1)	10813	The Preset Calibration is used to find the optimized preset for the platform.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 6 Instrument Names

Instrument Name	Description
JBERTA	N4903A High Performance Serial BERT
JBERTB	N4903B High Performance Serial BERT
scope	The primary oscilloscope

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